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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/762,074	01/29/2001	Douglas L. Jewell	2206-3750.1U	7836

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EXAMINER	
ENG, GEORGE	

ART UNIT	PAPER NUMBER
2643	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/762,074	JEWELL ET AL.	
	Examiner	Art Unit	
	George Eng	2643	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-12 and 14-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-12 and 14-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to amendment filed 7/7/2005. Accordingly claims 3, 13 and 21-24 are cancelled and claims 1-2, 4-12 and 14-20 are pending for examination

Claim Rejections - 35 USC § 112

2. Claims 1-2, 4-12 and 14-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1 and 11, each recites the limitations "said video decompression means", "said video receiving means", and "said video image out means" in line 3-4 on amendment page 3. There are insufficient antecedent bases for these limitations in the claims.

Claims 2 and 4-10, and 12 and 14-20 are also rejected because of depending on claims 1 and 11, respectively, containing the same deficiency.

Regarding claim 8 and 11, each recites the limitations "said encoding circuit" and "said decoding circuit" in lines 2-3. There are insufficient antecedent bases for these limitations in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-3, 5-6 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Palmer et al. (US PAT. 5,475,421 hereinafter Palmer).

Regarding claim 1, Applicant's admitted prior art as shown in figure 1 discloses a video conferencing circuit (12, figure 1) comprising video input device (26, figure 1), a remote interface circuit (22, figure 1), a video output device, and application specific integrated circuit (10, figure 1) connected to the video input device, to video output device and to remote interface device, the ASIC having a high speed serial interface video input (46, figure 1), a video-in circuit (24, figure 1) connected to the video input device to receive input video signal and the high speed serial data input, a memory circuit (14, figure 1) connected to the video-in circuit to receive the input video signal and the high speed serial video input, and the memory circuit being configured to retain and transmit the input video signal and the high speed serial video input as stored data, data compression circuit (34, figure 1) means connected to the memory circuit to

receive stored data and compress the stored data, a video decompression means (42, figure 1) operable to receive the incoming compressed data and configured to decompress and to transmit incoming compressed data to the memory circuit, video image output means (44, figure 1) connected to receive incoming stored data from the memory circuit and to transmit the incoming stored data to a display device, and video processing means (40, figure 1) connected to receive the outgoing compressed data and connected to the remote interface unit to transmit outgoing compressed data and to receive incoming compressed data from a remote station, said video processing means also being connected to the video-in circuit, the memory circuit, the video decompression means and the video image out means to control the flow of video signal therein between (see specification). Applicant's admitted prior art differs from the claimed invention in not specifically teaches video input means configured to select an input video signal from one of a plurality of video generating devices and the memory circuit being configured to convert the incoming compressed data to incoming stored data, wherein the memory circuit including a memory structure and a memory control circuit to convert the one of the input video signal and the high speed serial video input to stored data and to convert the incoming compressed data to incoming stored data. However, Palmer discloses a video teleconferencing workstation (12, figure 2) having a video frame grabber (34, figure 2) configured to select an input video signal from one ore more sources, i.e., a video camera (38, figure 2) and auxiliary video source (40, figure 2) and a video buffer control (35, figure 2) obviously including a memory structure and a memory control circuit to convert the video frame data to stored data in order to offer significantly increased system throughput and performance (col. 4 line 55 through col. 6 line 41). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the

invention was made to modify Applicant's admitted prior art in having video input means configured to select an input video signal from one of a plurality of video generating devices and the memory circuit being configured to convert the incoming compressed data to incoming stored data, wherein the memory circuit including a memory structure and a memory control circuit to convert the one of the input video signal and the high speed serial video input to stored data and to convert the incoming compressed data to incoming stored data, as per teaching of Palmer, in order to offer significantly increased system throughput and performance.

Regarding claim 2, Applicant's admitted prior art discloses the remote interface circuit (22, figure 1) includes a modem.

Regarding claim 4, Applicant's admitted prior art teaches the memory structure being a DRAM configured to receive and store the stored data and the incoming stored data (specification).

Regarding claim 5, Palmer discloses the video frame grabber to receive selected video signals and convert said selected video signals to an input video signal.

Regarding claim 6, Applicant's admitted prior art discloses the video-in circuit including control register connected to video processing means to receive control signals therefrom and Palmer teaches the video frame grabber having means connected to receive one of a plurality of video input signals and to operate to supply the one of the plurality of video input signals as input video signal to the video buffer (col. 5 lines 4-40). Thus, the combination of Applicant's admitted prior art and Palmer teaches the claimed limitations.

Regarding claims 8-9, Applicant's admitted prior art discloses a data bus (38, figure 1) for interconnecting between the video-in circuit, the memory circuit, the data compression

means, video decompression means and the video out circuit for transmitting control signals there between, and wherein the video processing means includes a bus control circuit (36, figure 1) connected to the data bus to supply the control signals thereto, wherein the bus control signal includes a bone interface circuit being configured to generate and supply the control signal (specification).

Regarding claim 10, Applicant's admitted prior art discloses video processor means (40, figure 4) includes a data processor connected to said remote interface circuit (22, figure 1) to supply and receive video signals to and from and external device for obtaining and displaying video images (specification) such that one skill in the art would recognize the video processor means further including the components as defined in the claim in order to perform such functions.

5. Claims 11-12, 14-15 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Palmer et al. (US PAT. 5,475,421 hereinafter Palmer) and Gould et al. (US PAT. 5,563,649 hereinafter Gould).

Regarding claim 11, Applicant's admitted prior art as shown in figure 1 discloses a video conferencing circuit (12, figure 1) comprising video input device (26, figure 1), a remote interface circuit (22, figure 1), a video output device, and application specific integrated circuit (10, figure 1) connected to the video input device, to video output device and to remote interface device, the ASIC having a high speed serial interface video input (46, figure 1), a video-in circuit (24, figure 1) connected to the video input device to receive input video signal and the high speed serial data input, a memory circuit (14, figure 1) connected to the video-in circuit to

receive the input video signal and the high speed serial video input, and the memory circuit being configured to retain and transmit the input video signal and the high speed serial video input as stored data, data compression circuit (34, figure 1) means connected to the memory circuit to receive stored data and compress the stored data, a video decompression means (42, figure 1) operable to receive the incoming compressed data and configured to decompress and to transmit incoming compressed data to the memory circuit, video image output means (44, figure 1) connected to receive incoming stored data from the memory circuit and to transmit the incoming stored data to a display device, and video processing means (40, figure 1) connected to receive the outgoing compressed data and connected to the remote interface unit to transmit outgoing compressed data and to receive incoming compressed data from a remote station, said video processing means also being connected to the video-in circuit, the memory circuit, the video decompression means and the video image out means to control the flow of video signal therein between (see specification). Applicant's admitted prior art differs from the claimed invention in not specifically teaches video input means configured to select an input video signal from one of a plurality of video generating devices and the memory circuit being configured to convert the incoming compressed data to incoming stored data, wherein the memory circuit including a memory structure and a memory control circuit to convert the one of the input video signal and the high speed serial video input to stored data and to convert the incoming compressed data to incoming stored data. However, Palmer discloses a video teleconferencing workstation (12, figure 2) having a video frame grabber (34, figure 2) configured to select an input video signal from one ore more sources, i.e., a video camera (38, figure 2) and auxiliary video source (40, figure 2) and a video buffer control (35, figure 2) obviously including a memory structure and a

memory control circuit to convert the video frame data to stored data in order to offer significantly increased system throughput and performance (col. 4 line 55 through col. 6 line 41). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Applicant's admitted prior art in having video input means configured to select an input video signal from one of a plurality of video generating devices and the memory circuit being configured to convert the incoming compressed data to incoming stored data, wherein the memory circuit including a memory structure and a memory control circuit to convert the one of the input video signal and the high speed serial video input to stored data and to convert the incoming compressed data to incoming stored data, as per teaching of Palmer, in order to offer significantly increased system throughput and performance. Furthermore, neither Applicant's admitted prior art nor Palmer specifically teaches video output means configured to select one of a plurality of video output devices to received an output video signal. However, Gould teaches a system capable of transmitting and receiving video material comprising means for converting received video depending upon the recipient's preference in order to make user friendly by allowing to select one of a plurality of output devices, i.e., a TV monitor or a high-resolution computer monitor, to receive an output video (abstract and col. 10 liens 48-65). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of the Applicant's admitted prior art and Palmer in having video output means configured to select one of a plurality of video output devices to received an output video signal, as per teaching of Gould, in order to make user friendly.

Regarding claim 12, Applicant's admitted prior art discloses the remote interface circuit (22, figure 1) includes a modem.

Regarding claim 14, Applicant's admitted prior art teaches the memory structure being a DRAM configured to receive and store the stored data and the incoming stored data (specification).

Regarding claim 15, Applicant's admitted prior art discloses the video-in circuit including control register connected to video processing means to receive control signals therefrom and Palmer teaches the video frame grabber having means connected to receive one of a plurality of video input signals and to operate to supply the one of the plurality of video input signals as input video signal to the video buffer (col. 5 lines 4-40). Thus, the combination of Applicant's admitted prior art and Palmer teaches the claimed limitations.

Regarding claims 17-18, Applicant's admitted prior art discloses a data bus (38, figure 1) for interconnecting between the video-in circuit, the memory circuit, the data compression means, video decompression means and the video out circuit for transmitting control signals there between, and wherein the video processing means includes a bus control circuit (36, figure 1) connected to the data bus to supply the control signals thereto, wherein the bus control signal includes a bone interface circuit being configured to generate and supply the control signal (specification).

Regarding claim 19, Applicant's admitted prior art discloses video processor means (40, figure 4) includes a data processor connected to said remote interface circuit (22, figure 1) to supply and receive video signals to and from and external device for obtaining and displaying video images (specification) such that one skill in the art would recognize the video processor

means further including the components as defined in the claim in order to perform such functions.

Allowable Subject Matter

6. Claims 7, 16 and 20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 1-2, 4-12 and 14-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Eng whose telephone number is (571) 272-7495. The examiner can normally be reached on Tue-Fri 7:30 AM-6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis A. Kuntz can be reached on (571) 272-7499. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Eng
Primary Examiner
Art Unit 2643